Digital Logic Design

Project

Topic:

4-bit Even, Odd AND

Prime number detector

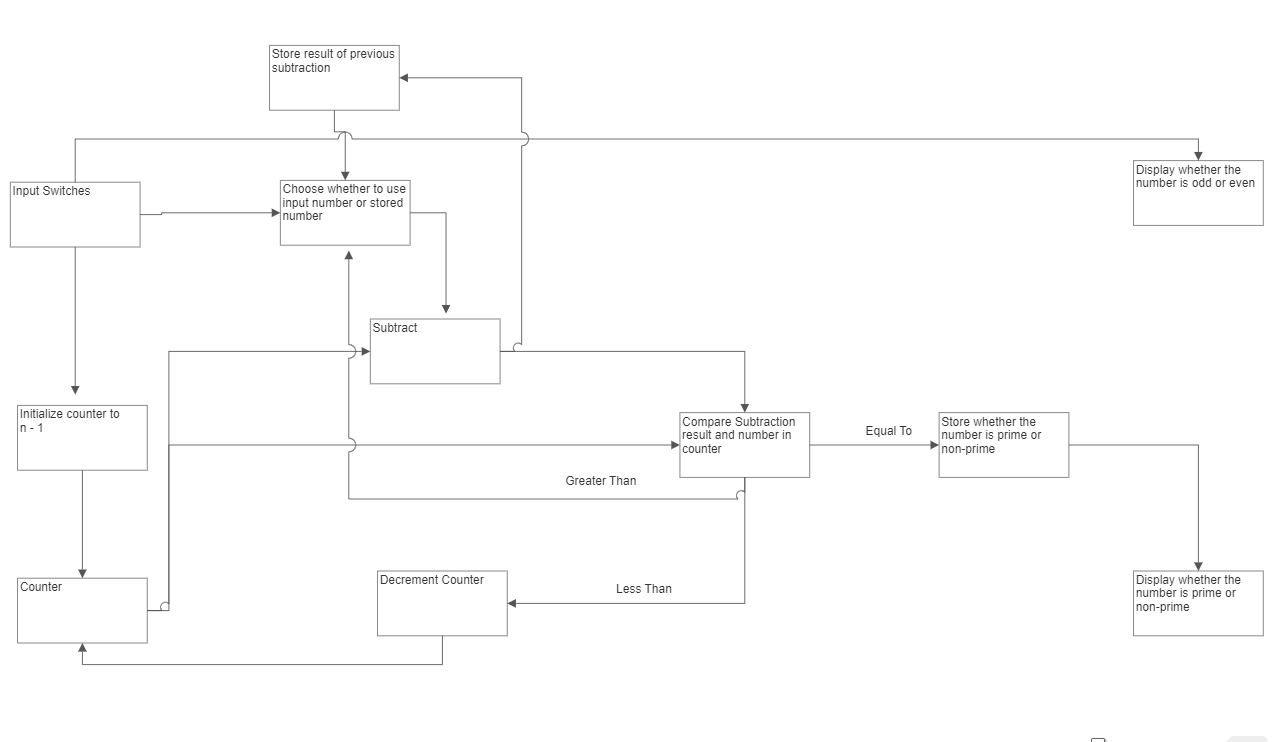
Abdul Rehman Ansari

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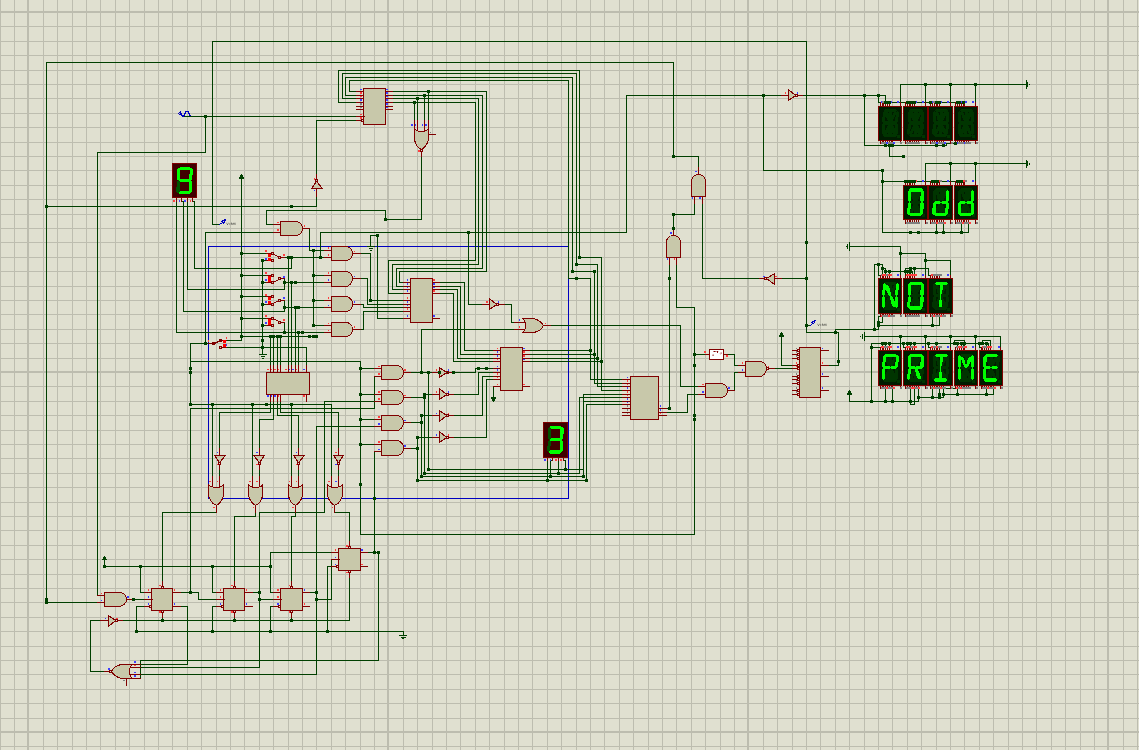
Components Used:

* 4-bit Adders (74LS83)
* Switches (SW-SPDT)
* AND Gates (74LS08)
* OR Gates (74LS32)
* NOT Gates (74LS04)
* NAND Gates (74LS26)
* 4-input NOR gate (7425)
* 7 Segment Displays (To Display input number and current number in counter)
* 14 segment Displays
* Hex D Flip Flops with Reset (74HCT174)
  + Used instead of its TTL replacement due to Technical issues
* 4-bit Comparator (74LS85)
* OP : Delay
  + Delays signal (used to better synchronize output with input)
* Quad S-R Latches (74LS279)
* Digital Clock
* J-K Flip Flops with Set and Reset (74LS109)

Block Diagram:



Circuit Diagram:



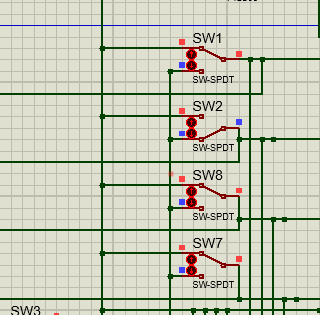
Methodology:

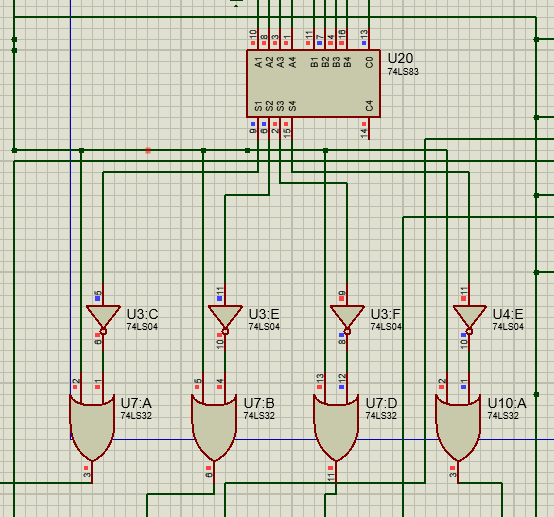
1. A number (n) will be taken as input from the user.
2. To Check whether n is prime or not prime, the circuit will compute a remainder when n is divided by numbers n-1 to 2.
3. If at any point, the remainder is found to be 0, a flag will be raised to signify that n is not a prime number.
4. If we have reached 1 and the remainder has not reached 0 even once, n will be found to be prime

For Even and Odd numbers, the Least Significant Bit (LSB) of input is checked

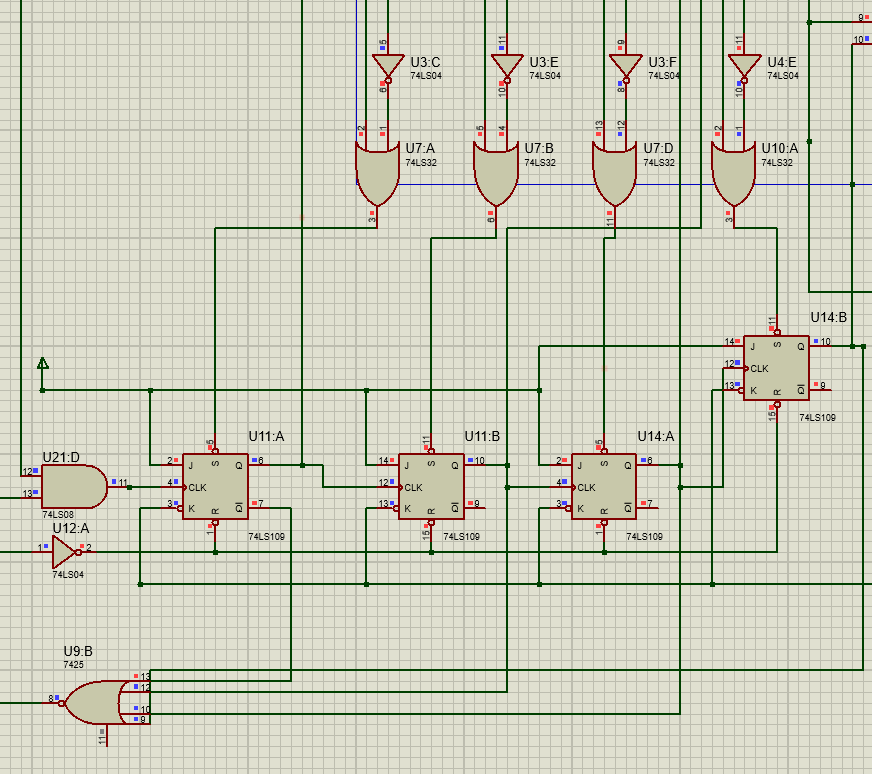
1. If it is 1, the number is odd.
2. If it is 0, the number is even.

Circuit Explanation:

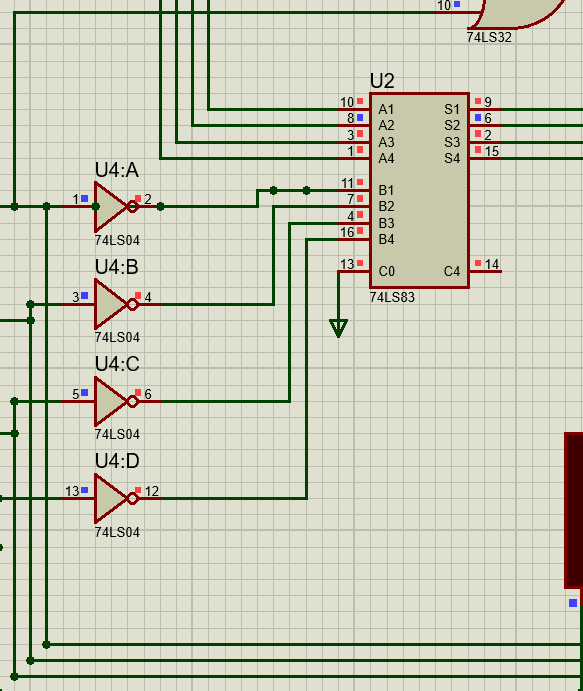
1. Input a 4-bit binary number using Switches (suppose input = n)
2. 1 is subtracted from the n using 2s compliment to obtain the number that will be repeatedly subtracted from n first.



1. That number is stored in a series of flip flops (Used to make a down counter) using the set pins of the flip flops
   1. To ensure that the number is set only once, an arrangement of OR and NOT gates is used to generate a short pulse from a long signal (that lasts till the end of the circuit )

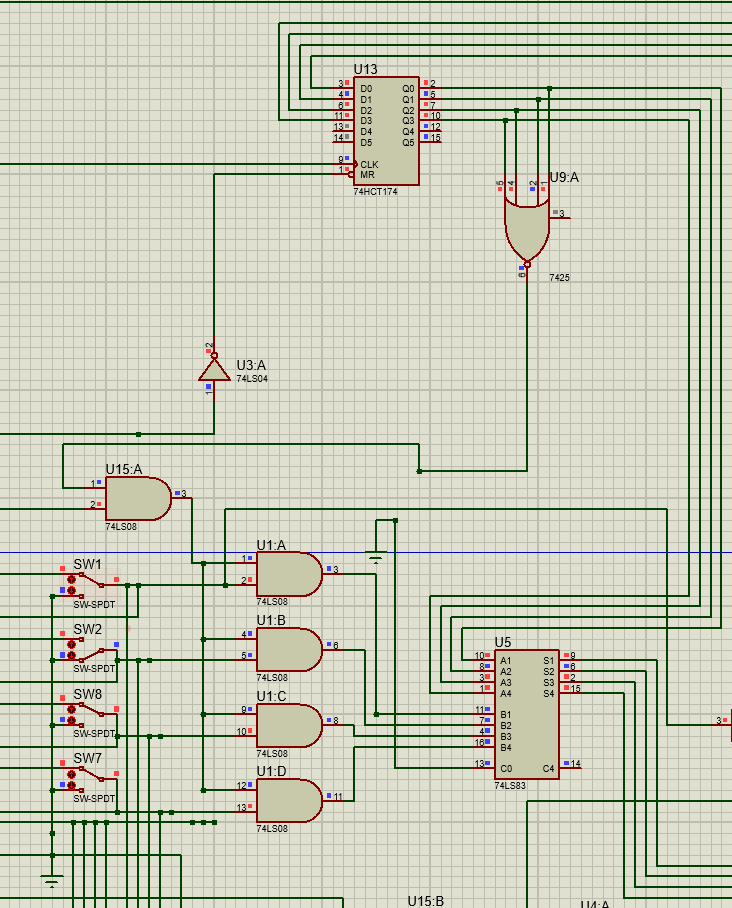


1. Once the counter has been setup, the first subtraction takes place by using a 4-bit adder to add the input n and 2s compliment of the number in the counter

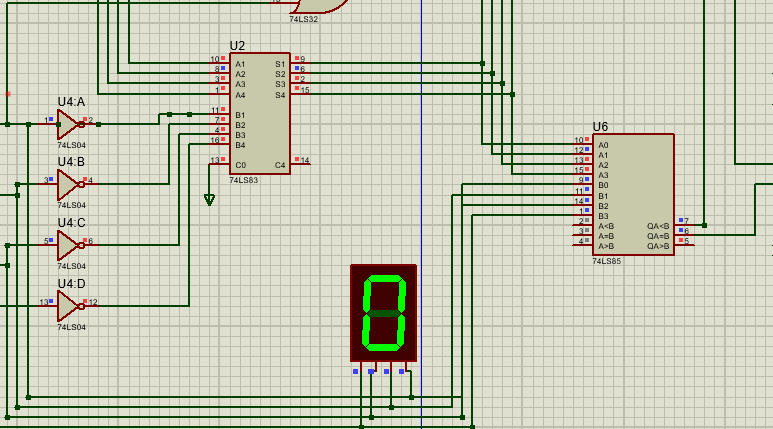


1. To perform the repeated subtraction, the result of the first subtraction is stored in a 4 d flip flops. For the second subtraction, the number stored in the flip flops will be used instead of the input number. This is done by checking if the number in the flip flops is zero using a 4-input NOR gate.
   1. If it is zero, the input number is added into the stored number resulting in the input number itself.
   2. If it is not zero, the input number is Anded with the result of the NOR gate which is 0. This makes the input number 0. The input number and the stored numbers are again added resulting in the stored number.

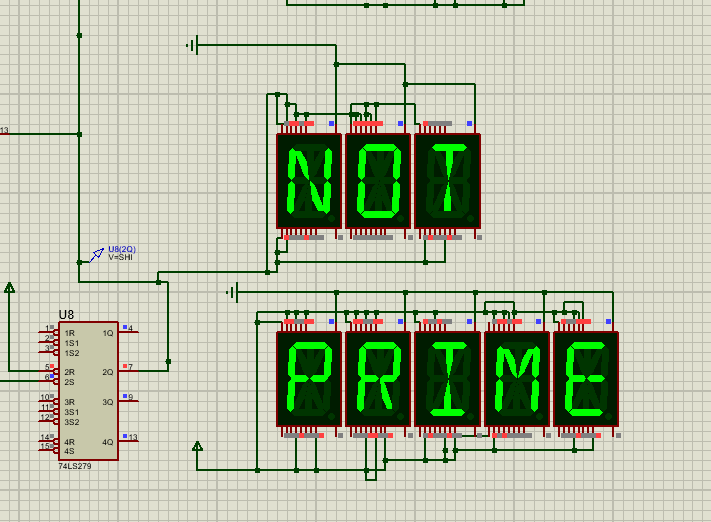
A clock is also used to manage a synchronous operation. This Clock is used in all modules to ensure that the output is reliable.



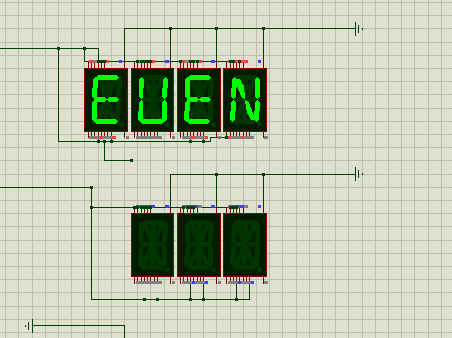
1. After every subtraction. A comparator is used to check whether the result of the subtraction is lower, equal or greater than the number in the counter.
   1. If it is lower, then the remainder is not zero. So the stored number is reset to 0 and the counter is decremented by one.
   2. If it is equal, then the remainder is zero. So a S-R latch is set to SET mode (previously set to RESET MODE on circuit start)
   3. If it is greater, then no conclusion can be derived and further subtractions need to take place. So no action is taken



1. The S-R latch is fed into an array of 14 segment displays that says PRIME when the number is prime and NOT PRIME when the number is not prime.



1. Similarly, an array of 14 segment displays also display whether the number is odd or even.



Data Sheets:

